

What is claimed is:

1 1. A cache-coherent device comprising:
2 a plurality of client ports, each to be coupled to one of a plurality of port components;
3 a plurality of sub-unit caches, each coupled to one of said plurality of client ports and
4 assigned to one of said plurality of port components; and
5 a coherency engine coupled to said plurality of sub-unit caches.

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4 a cache-coherent device coupled to said processor and including a plurality of client
5 ports, each coupled to one of said plurality of port components, said cache-coherent device
6 further including a plurality of caches, each coupled to one of said plurality of client ports and
7 assigned to one of said plurality of port components, and a coherency engine coupled to said
8 plurality of caches.

1 7. The processing system of claim 6 wherein said plurality of port components include
2 processor port components.

3 8. The processing system of claim 6 wherein said plurality of port components include
4 input/output components.

5 9. In a cache-coherent device including a coherency engine and a plurality of client ports, a
6 method for processing a transaction, comprising:

7 receiving a transaction request at one of said plurality of client ports, said transaction
8 request includes an address; and

9 determining whether said address is present in one of a plurality of sub-unit caches, each
10 of said sub-unit caches assigned to said of a plurality of client ports.

1 10. The method of claim 9 wherein said transaction request is a read transaction request.

1 11. The method of claim 10 further comprising:

transmitting data for said read transaction request from said one of said plurality of sub-unit caches to one of said plurality of client ports.

12. The method of claim 11 further comprising:
prefetching one or more cache lines ahead of said read transaction request; and
updating the coherency state information in said plurality of sub-unit caches.

13. The method of claim 12 wherein the coherency state information includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol.

14. The method of claim 9 wherein said transaction request is a write transaction request.

15. The method of claim 14 further comprising:
modifying coherency state information for a cache line in said one of said plurality of sub-unit caches;
updating coherency state information in others of said plurality of sub-unit caches by said coherency engine; and
transmitting data for said write transaction request from said one of said plurality of sub-unit caches to memory.

16. The method of claim 15 further comprising:
modifying coherency state information of said write transaction request in the order received; and

4 pipelining multiple write requests.

1 17. The method of claim 16 wherein the coherency state information includes a Modified-
2 Exclusive-Shared-Invalid (MESI) cache coherency protocol.

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